

WHAT IS CLAIMED IS:

- 1 1. A method of operating an integrated circuit including
2 read accessible memory comprising the steps of:
3 testing memory read operations beginning at a maximum
4 speed at successively slower speeds until all memory reads
5 pass;
6 determining memory read program bits for a highest memory
7 speed passing the memory read tests; and
8 programming write once bits according to determined
9 memory read program bits.
- 1 2. The method of claim 1 further comprising the steps
2 of:
3 preliminary soft programming determined bits; and
4 testing non-memory portions of the integrated circuit
5 using soft programmed determined memory read program bits.
- 1 3. The method of claim 1 wherein:
2 said step of programming write once bits includes
3 applying program voltages to the bits,
4 testing the write once bits to determine achieved
5 programming, and
6 repeating applying program voltages and testing the
7 write once bits until the testing confirms correct write
8 once bit programming.

1 4. The method of claim 1 wherein programming of eFuse
2 bits includes:

3 merging of programming of write once bits for memory read
4 speed with programming write once bits not related to memory
5 speed.

1 5. The method of claim 4 wherein:

2 the write once bits not related to memory speed include a
3 specific die-identification bit code.

1 6. The method of claim 4 wherein:

2 the write once bits not related to memory read speed
3 include write once bits for memory redundancy programming.

1 7. The method of claim 4 wherein:

2 the write once bits not related to memory read speed
3 include write once bits for control of programmable logic
4 functions.

1 8. The method of claim 1, wherein the read accessible
2 memory is write accessible, further comprising:

3 testing memory write operations beginning at a maximum
4 speed at successively slower speeds until all memory reads
5 pass;

6 determining memory write program bits for a highest
7 memory speed passing the memory write tests; and

8 said step of programming write once bits according to
9 determined memory read program bits further includes
10 programming write once bits according determined memory write
11 program bits.

1 9. A method of operating an integrated circuit including
2 write accessible memory comprising the steps of:
3 testing memory write operations beginning at a maximum
4 speed at successively slower speeds until all memory writes
5 pass;
6 determining memory write program bits for a highest
7 memory speed passing the memory write tests; and
8 programming write once bits according to determined
9 memory write program bits.

1 10. The method of claim 9 further comprising the steps
2 of:
3 preliminary soft programming determined write once bits;
4 and
5 testing non-memory portions of the integrated circuit
6 using soft programmed determined memory write program bits.

1 11. The method of claim 9 wherein:
2 said step of programming write once bits includes
3 applying program voltages to the write once bits,
4 testing the write once bits to determine achieved
5 programming, and
6 repeating applying program voltages and testing the
7 write once bits until the testing confirms correct write
8 once bit programming.

1 12. The method of claim 9 wherein:
2 programming of write once bits includes merging of
3 programming of write once bits for memory write speed with
4 programming write once bits not related to memory speed.

1 13. The method of claim 12 wherein:
2 the write once bits not related to memory write speed
3 include a specific die-identification bit code.

1 14. The method of claim 12 wherein:
2 the write once bits not related to memory write speed
3 include write once bits for memory redundancy programming.

1 15. The method of claim 12 wherein:
2 the write once bits not related to memory write speed
3 include write once bits for control of programmable logic
4 functions.

1 16. An integrated circuit comprising:
2 a plurality of write once bits including at least one
3 read timing write once bit and at least one write timing write
4 once bit;
5 a logic circuit;
6 a read/write memory connected to said write once bits and
7 said logic circuit, said read/write memory operable to read
8 data from memory locations specified by said logic circuit and
9 write data to memory locations specified by said logic
10 circuit, said read/write memory including
11 a read timing circuit selecting one of a plurality
12 of intervals of time from a start of read operations
13 until sampling of read data dependent upon said at least
14 one read timing write once bit, and
15 a write timing circuit selecting one of a plurality
16 of intervals of time of application of write data to said
17 corresponding memory locations dependent upon said at
18 least one write timing write once bit.

1 17. The integrated circuit of claim 16, wherein:
2 said logic circuit includes a programmable data
3 processor.

1 18. The integrated circuit of claim 16, further
2 comprising:
3 a plurality of data bit latches, one data bit latch
4 corresponding to each of said write once bits;
5 wherein said reading timing circuit is responsive to said
6 data bit latches corresponding to said at least one read
7 timing write one bit in a test mode; and
8 wherein said write timing circuit is responsive to said
9 data bit latches corresponding to said at least one write
10 timing write one bit in a test mode.